Claims

What is claimed is:

1. A multi-element floating gate for an EEPROM comprising:

a main polysilicon body disposed over a semiconducting substrate and electrically insulated therefrom in a first active region;

source and drain implants within the semiconducting substrate on opposed sides of the main polysilicon body, the drain implant having a size exceeding the source implant;

a polysilicon spacer disposed over the semiconducting substrate and electrically insulated therefrom and spaced from the main polysilicon body by a layer of thin oxide, the thin oxide extending over the main polysilicon body, all in the first active region;

a polysilicon cap disposed over the polysilicon spacer in electrical contact therewith and disposed over the thin oxide on the main polysilicon body, the polysilicon cap having a metal filled hole through the cap and through the main polysilicon body whereby metal in the hole electrically joins the main polysilicon body with the polysilicon spacer;

a second active region having an implanted region, the second active region insulated from the first active region, said drain implant electrically extending to the implanted region in the second active region wherein a charge storage reservoir is provided for programming.

2. The device of claim 1 wherein the polysilicon spacer surrounds the main polysilicon body.

3. The device of claim 1 where the semiconducting substrate has at least one of the source and drain implants beneath the polysilicon spacer.

4. The device of claim 1 wherein said second active region is smaller than the first active region.

5. The device of claim 1 wherein the implanted region in the second active region occupies the entire second active region.

6. The device of claim 5 wherein said charge storage reservoir associated with the second active region is larger than in the first active region.

7. A method of making a multi-element floating gate for an EEPROM comprising:

depositing a first polysilicon layer over a semiconducting substrate and electrically insulated therefrom and etching away polysilicon leaving a main polysilicon body;

depositing a second polysilicon layer in an insulated relation over the main polysilicon body and the etching away the polysilicon, leaving a polysilicon spacer near the main polysilicon body, electrically insulated from the substrate and spaced from the main polysilicon body by a layer of thin oxide, the thin oxide extending over the main polysilicon body;

depositing a third polysilicon layer over the polysilicon spacer and in electrical contact therewith and over thin oxide on the main polysilicon body;

forming a hole in the polysilicon cap through the cap and through the main polysilicon body, filling said hole with conductive material whereby conductive material in the hole electrically joins the main polysilicon body with the polysilicon spacer.

8. The method of claim 7 further defined by implanting charged particles into the semiconducting substrate using the main polysilicon body as an alignment mask.

9. The method of claim 8 further defined by connecting the implanted charged particles as source and drain regions relative to the main polysilicon body.

10. The method of claim 8 wherein the second polysilicon layer is deposited after the implanting of charged particles.

11. A method of making a floating gate EEPROM device comprising:

defining first and second mutually isolated active areas on a semiconductor substrate;

forming a conductive, electrically floating, polysilicon region in the first active area, separated from the substrate by a corresponding areawise region of gate oxide, with a common pair of opposed edges over the substrate;

implanting source and drain regions in the substrate self-aligned with the opposed edges of the polysilicon region, the drain region being larger than

the source and extending from the first active region into the second active region;

forming conductive, electrically floating poly spacers near opposed edges of the conductive polysilicon region and over the source and drain regions, separated from the source and drain regions and from the polysilicon region by a layer of tunnel oxide, thereby forming a mesa feature over the substrate;

covering the mesa feature with a capping dielectric layer;

depositing a polysilicon layer over the capping dielectric layer;

making a hole in the mesa feature penetrating polysilicon layer;

filling the hole with conductive material, thereby electrically joining the poly spacers to the conductive region and forming a single floating gate.

12. The method of claim 11 further defined by selectively doping the substrate in a region forming a portion of the second active region prior to forming the conductive, electrically floating polysilicon region.

13. The method of claim 11 wherein the electrically floating, polysilicon region in the first active area is formed by depositing a first polysilicon layer over the substrate, separated therefrom by oxide and etching away polysilicon except for said polysilicon region.

14. The method of claim 13 wherein the conductive, electrically floating polysilicon region is formed by depositing a second layer of polysilicon layer over the substrate and said polysilicon region, separated therefrom by oxide and etching away polysilicon except for the floating spacers.

15. The method of claim 14 wherein the conductive, electrically floating spacers are formed by depositing a third layer polysilicon layer over the floating spacers and the polysilicon region, separated therefrom by oxide.